FPGA IMPLEMENTATION OF DIFFERENT MULTIPLIER ARCHITECTURES

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ABSTRACT

In this paper 2 different multiplier architectures are implemented in Xilink FPGA and compared for their performance. Here these architectures are implemented for 4,8,16 bit

Based on various speed- up schemes for binary multiplication, a comprehensive overview of different multiplier architectures are given in this report. In addition , it is found that booth multiplier is faster than array multiplier.

KEYWORDS: Multiplier, Computer Arithmetic Algorithm, FPGA